REMARKS

Applicant respectfully requests reconsideration and allowance of the subject application. Claims 1-13 are pending, of which claims 1 and 13 have been amended. The amendments to claims 1 and 13 are simply to correct informalities, and are not to overcome prior art.

35 U.S.C. §112 Claim Rejections

Claims 1-6 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite (*Office Action* p.2). An appropriate correction to claim 1 has been provided herein, and Applicant respectfully requests that the §112 rejection of claims 1-6 be withdrawn.

35 U.S.C. §102 Claim Rejections

Claims 1-2, 6-8, and 10-11 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,594,796 to Chiang (hereinafter, "Chiang") (*Office Action* p.3). Applicant respectfully traverses the rejection.

Claim 1 recites a method of performing parity operations in a redundant data storage system. Chiang does not show or disclose any such redundant data storage system to store data in a redundant configuration. The Office characterizes Chiang as disclosing a memory array (11, Fig. 1) "in a redundant data storage system" (*Office Action* p.3). Applicant disagrees because Chiang only describes a single memory from which data elements are read (col.2, lines 25-26; item 11, Fig. 1).

Claim 1 also recites that "there are different parity operations involving different subsets of the parity coefficients", the method comprising "pre-selecting parity coefficient subsets for use in the different parity

operations". Chiang does not show or disclose different parity operations, or parity coefficient subsets, as recited in claim 1. The Office states that Chiang discloses "different parity operations, such as parity error generation" (*Office Action* p.3). Applicant disagrees that Chiang discloses parity operations other than the reference to error detection.

Chiang describes a procedure to read data only once from memory which is then received by an EDC processor unit, an ECC-P parity processor unit, and an ECC-Q parity processor unit (col.1, lines 35-39; col.2, lines 25-29). The processor units generate an error detection control, P-parity coefficients, and Q-parity coefficients. Other than generating the parity coefficients, Chiang does not disclose any other parity operations.

Claim 1 also recites storing "the pre-selected parity coefficient subsets in a memory". Chiang does not show or disclose parity coefficient subsets, as recited in claim 1. Applicant describes, as one example, that parity coefficient subsets 31 (Fig. 3) are stored as a P-parity segment and a Q-parity segment together in a classification 32 (*Specification* p.10, lines 17-24). Chiang only describes generating parity coefficients that are held in memory (Fig. 13).

Claim 1 also recites "performing the particular parity operation with the subset of parity coefficients that was read from the memory." Chiang does not indicate performing a parity operation with a subset of parity coefficients, as recited in claim 1. Chiang only describes generating parity coefficients, but not parity coefficient subsets or performing a parity operation with a subset of parity coefficients.

The Office states that Chiang discloses "performing the particular parity operation with the subset of parity coefficients (s0 and s0') that was read from the memory." (*Office Action* p.4). Applicant disagrees that Chiang discloses reading a subset of parity coefficients from memory or performing a parity

operation with the subset of parity coefficients. Further, the Office does not provide an indication as to which feature(s) in Chiang are being relied upon to reject performing a parity operation with a subset of parity operations that was read from memory, as recited in claim 1.

Accordingly, claim 1 is allowable over Chiang for the several reasons described above, and Applicant respectfully requests that the §102 rejection be withdrawn.

Claims 2 and 6 are allowable by virtue of their dependency upon claim 1. Additionally, claim 6 is allowable over Chiang for independent reasons.

Claim 6 recites "packing the groups of subsets in order of increasing subset size in a linear memory array", "calculating an offset in the linear memory array of a particular group *i* corresponding to a subset size L_i", and "reading a subset of values from the particular group corresponding to the subset size of L_i at the calculated offset in the linear memory array."

As described above in the response to the rejection of claim 1, Chiang does not show or disclose parity coefficient subsets. Further, Chiang does not show or disclose packing the groups of subsets in order of increasing subset size in a linear memory array, or calculating an offset in the linear memory array, as recited in claim 6. The Office states that Chiang discloses "calculating an offset, such as index "k", by receiving the data element value s(k)" (*Office Action* p.4). However, the sequence number "k" simply identifies data elements in a serial order (col.1, lines 42-47). There is no indication in Chiang of calculating an offset in a linear memory array, as recited in claim 6.

There is also no indication in Chiang of subset size or packing the groups of subsets in order of increasing subset size, as recited in claim 6.

Further, the Office does not provide an indication as to which feature(s) in Chiang are being relied upon to reject packing the groups of subsets in order of increasing subset size, as recited in claim 6.

Chiang also does not show or disclose reading a subset of values from the particular group corresponding to the subset size of L_i at the calculated offset in the linear memory array, as recited in claim 6. Further, the Office does not provide an indication as to which feature(s) in Chiang are being relied upon to reject this element of claim 6.

Accordingly, claim 6 is allowable over Chiang and Applicant respectfully requests that the §102 rejection be withdrawn.

Claim 7 recites a method of accessing pre-selected subsets of values comprising "packing the groups of subsets in order of increasing subset size in a linear memory array", "calculating an offset in the linear memory array of a particular group *i* corresponding to a subset size L_i in accordance with a predefined function of N and L_i", and "reading a subset of values from the particular group *i* at the calculated offset in the linear memory array."

Chiang does not show or disclose these features recited in claim 7. As described above in the response to the rejection of claim 6, there is no indication in Chiang of packing groups of subsets in order of increasing subset size in a linear memory array, or reading a subset of values from a particular group *i* at the calculated offset in the linear memory array, as recited in claim 7. Further, the Office does not provide an indication as to which feature(s) in Chiang are being relied upon to reject packing the groups of subsets in order of increasing subset size, and reading a subset of values at the calculated offset, as recited in claim 7.

Chiang also does not show or disclose calculating an offset in the linear memory array, as recited in claim 7. The Office states that Chiang discloses "calculating an offset, such as index "k", by receiving the data element value s(k)" (*Office Action* p.4). However, the sequence number "k" simply identifies data elements in a serial order (col.1, lines 42-47). There is no indication in Chiang of calculating an offset in a linear memory array, as recited in claim 7.

Accordingly, claim 7 along with dependent claim 8 is allowable over Chiang and Applicant respectfully requests that the §102 rejection be withdrawn.

Claim 10 is rejected with claim 1 (*Office Action* p.3). However, for the many reasons described above in response to the rejection of claim 1, claim 10 is allowable over Chiang. For example, claim 10 recites "a disk controller that performs parity operations in a redundant data storage system". Chiang does not show or disclose any such redundant data storage system to store data in a redundant configuration. The Office characterizes Chiang as disclosing a memory array (11, Fig. 1) "in a redundant data storage system" (*Office Action* p.3). Applicant disagrees because Chiang only describes a single memory from which data elements are read (col.2, lines 25-26; item 11, Fig. 1).

Claim 10 also recites that there are "different parity operations involving different subsets of parity coefficients", and "stored subsets of parity coefficients corresponding respectively to different parity-related computation scenarios". Chiang does not show or disclose different parity operations, or stored subsets of parity coefficients corresponding respectively to different parity-related computation scenarios", as recited in claim 10. The Office states that Chiang discloses "different parity operations, such as parity error generation" (*Office Action* p.3). As described above in the response to the

rejection of claim 1, Applicant disagrees that Chiang discloses parity operations other than the reference to error detection.

Claim 10 also recites "reading the corresponding subset of parity coefficients from the memory", and "performing the particular parity-related operation with the subset of parity coefficients read from the memory." Chiang does not show or disclose reading a subset of parity coefficients from memory, as recited in claim 10. Chiang only discloses generating parity coefficients which are then held in memory (col.14, lines 25-28). There is no indication in Chiang of then reading the coefficients from memory or of performing a parity-related operation with the coefficients, as recited in claim 10.

Accordingly, claim 10 is allowable over Chiang and Applicant respectfully requests that the §102 rejection be withdrawn.

Claim 11 is allowable by virtue of its dependency upon claim 10. Additionally, claim 11 is allowable over Chiang for independent reasons. Claim 11 recites that "the stored subsets are indexed within the memory." As described above in the response to the rejection of claim 6, the Office states that Chiang discloses "calculating an offset, such as index "k", by receiving the data element value s(k)" (*Office Action* p.4). However, the sequence number "k" simply identifies data elements in a serial order (col.1, lines 42-47). There is no indication in Chiang that subsets are stored indexed within the memory, as recited in claim 11.

Accordingly, claim 11 is allowable over Chiang and Applicant respectfully requests that the §102 rejection be withdrawn.

35 U.S.C. §103 Claim Rejections

Claims 3-5 and 12-13 are rejected under 35 U.S.C. §103(a) for obviousness over Chiang in view of U.S. Patent No. 5,819,109 to Davis (hereinafter, "Davis") (*Office Action* p.5). Applicant respectfully traverses the rejection.

Claims 3-5 are allowable by virtue of their dependency upon claim 1 which is allowable over Chiang as described above in the response to the §102 rejection of claim 1. Additionally, claims 3-5 are allowable over the Chiang-Davis combination.

Claims 3-5 recite "classifying the different parity operations into classifications comprising parity segment generation operations, parity segment regeneration operations, and data segment reconstruction operations", and "each classification scenario involving a respective set of parity coefficients".

Chiang and/or Davis do not teach or suggest the parity operation classifications as recited in claims 3-5. Chiang describes generating parity coefficients and code words. However, there is no indication in Chiang of parity segment regeneration or of data segment reconstruction operations, as recited in claims 3-5. The Office recognizes that Chiang does not disclose data segment reconstruction operations (*Office Action* p.6).

The Office states that Chiang discloses parity segment generation and parity segment regeneration as shown in Figs. 9-12 (*Office Action* p.5). Applicant disagrees because Chiang states that "Figs. 9, 10, 11, and 12 illustrate suitable apparatus for processing the data elements" to determine parity checkbytes according to a second embodiment (col.10, lines 29-33). Chiang Figs. 1-8 are described relative to a first embodiment to read data only once from memory and generate an error detection control, P-parity

coefficients, and Q-parity coefficients. Chiang Figs. 9-12 are merely a second embodiment to generate the error detection control, P-parity coefficients, and Q-parity coefficients. There is no indication in Chiang of parity segment regeneration, as characterized by the Office.

Davis also does not teach or suggest parity segment regeneration, and there is no indication from the Office that Davis does. Accordingly, claims 3-5 are allowable over the Chiang-Davis combination and Applicant respectfully requests that the §103 rejection be withdrawn.

Claims 12-13 are allowable by virtue of their dependency upon claim 10 which is allowable over Chiang as described above in the response to the §102 rejection of claim 10. Additionally, claims 12-13 are allowable over the Chiang-Davis combination.

Claims 12-13 recite that "the parity-related computation scenarios are classified under classifications comprising parity segment generation operations, parity segment regeneration operations, and data segment reconstruction operations".

As described above in the response to the rejection of claims 3-5, claims 12-13 are allowable over the Chiang-Davis combination and Applicant respectfully requests that the §103 rejection be withdrawn.

Claim 9 Not Substantively Rejected

The Office Action Summary indicates that claims 1-13 are rejected. However, there is no discussion pertaining to a rejection of claim 9 and Applicant is unable to formulate a detailed response.

Claim 9 (dependent upon claim 7) recites "within any individual group *i*, calculating a memory offset of a subset D in the individual group as a function

of subset size L_i." Based on the above discussion, and as described above in the response to the rejection of claim 7, Chiang does not disclose calculating a memory offset, as recited in claim 9. Accordingly, Applicant respectfully requests that claim 9 be allowed.

Conclusion

Pending claims 1-13 are in condition for allowance. Applicant respectfully requests reconsideration and issuance of the subject application. If any issues remain that preclude issuance of this application, the Examiner is urged to contact the undersigned attorney before issuing a subsequent Action.

Respectfully Submitted,

Dated: April 27, 2004 By: _____

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